LISTING OF THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application. Where claims have been amended and/or canceled, such amendments and/or cancellations are done without prejudice and/or waiver and/or disclaimer, and the right to claim this subject matter in a continuing application is hereby reserved.

1. (Currently Amended) A system for processing an input signal, the system comprising:

- a predistortion subsystem ~~for receiving~~ adapted to receive said input signal and ~~for producing~~ adapted to produce a predistorted signal by applying a deliberate predistortion to said input signal, wherein said predistortion subsystem is adapted to distort said input signal to compensate for distortions in a system output signal; and

- a signal processing subsystem adapted to receive ~~receiving~~ and ~~processing~~ process said predistorted signal and adapted to produce ~~producing~~ a system output signal, wherein [[-]]~~said predistortion subsystem distorts said input signal to compensate for distortions in said system output signal;~~ [[-]]said signal processing subsystem ~~decomposes~~ is adapted to decompose said predistorted signal into separate components, each of said separate components being processed separately; and [[-]]said signal processing subsystem ~~combines~~ is adapted to combine said components after processing to produce said system output signal; and wherein said signal processing subsystem comprises:

a signal decomposer adapted to decompose said predistorted signal into at least two components, each of the at least two components exhibiting a phase and a magnitude, the magnitude of at least two of the at least two component signals being substantially equal;

at least two signal component processor blocks, each of said at least two signal component processor blocks including an amplifier, each signal processor block adapted to receive an output from said signal decomposer and each signal processor block adapted to separately process said output received from said signal decomposer; and

a combiner adapted to receive a processed output from each of said at least two signal component processor blocks, said combiner producing said system output signal from said processed outputs of said at least two signal component processor blocks.

2. (Cancelled) A system according to claim 1 wherein said signal processing subsystem comprises:

- a signal decomposer for decomposing said predistorted signal into at least two components;

- at least two signal component processor blocks, each signal processor block receiving an output of said signal decomposer and each signal processor block separately processes said output received from said signal decomposer; and

- a combiner receiving a processed output from each of said at least two signal component processor blocks, said combiner producing said system output signal from said processed outputs of said at least two signal component processor blocks.

3. (Cancelled) A system according to claim 2 wherein at least one of said at least two signal component processor blocks includes an amplifier.

4. (Currently Amended) A system according to claim [[3]] 1 wherein said amplifier ~~is~~ comprises a non-linear amplifier.

5. (Original) A system according to claim 1 wherein said system is part of a signal transmission system.

6. (Original) A system according to claim 1 wherein at least some of said distortions are due to said combiner.

7. (Currently Amended) A system according to claim [[3]] 1 wherein said amplifier ~~is~~ comprises a switch mode amplifier.

8. (Currently Amended) A system according to claim [[3]] 1 wherein said amplifier has a low-output impedance.

9. (Currently Amended) A system according to claim 1 wherein said deliberate predistortion includes magnitude distortions ~~which~~ adapted to adjust a magnitude of said input signal.

10. (Currently Amended) A system according to claim 1 wherein said deliberate predistortion includes phase distortions ~~which~~ adapted to adjust a phase of said input signal.

11. (Original) A system according to claim 1 wherein said deliberate predistortion is based on at least one entry in a lookup table.

12. (Currently Amended) A method of processing an input signal to produce a system output signal, the method comprising:

~~a)~~ receiving said input signal;

~~b)~~ applying a deliberate predistortion to said input signal to ~~result in~~ provide a predistorted signal;

~~c)~~ decomposing said predistorted signal into at least two component signals; each of the at least two component signals exhibiting a phase and a magnitude, the magnitude of at least two of the at least two component signals being substantially equal;

separately processing each of said at least two component signals, wherein said processing further includes amplifying each of said at least two component signals; and

~~d)~~ combining said at least two component signals to produce said system output signal.

13. (Original) A method according to claim 12 wherein said system output signal is an RF modulated version of said input signal.

14. (Cancelled) A method according to claim 12 further including a processing step of separately processing each of said at least two component signals prior to step d).

15. (Cancelled) A method according to claim 14 wherein said processing step includes amplifying at least one of said at least two component signals.

16. (Currently Amended) A method according to claim [[14]] 12 wherein said processing ~~step~~ includes phase modulating at least one of said at least two component signals.

17. (Currently Amended) A method according to claim 12 wherein ~~step a)~~ said receiving further includes ~~the step of~~ accessing an entry in a lookup table, said deliberate predistortion being ~~bases~~ based, at least in part, on said entry.

18. (Original) A method according to claim 17 wherein said deliberate predistortion is based on an interpolation of entries in said table.

19. (Original) A system according to claim 11 wherein said deliberate predistortion is based on an interpolation of entries in said table.